REMARKS

By the above amendment, independent claim 3 has been amended to clarify the fact that the holding of the wafer at a position corresponding to the upper member of the stage for a predetermined time period is effected without mounting of the wafer on the upper member of the stage, which feature is considered to be inherent in that the following step recites mounting the wafer on the upper member of the stage. Claim 3 has also been amended to recite the feature that the mounting of the wafer on the upper member of the stage enables processing of the wafer which is mounted on the upper member of the stage by using the plasma in the vacuum chamber. Furthermore, dependent claims 4 and 7 have been amended to indicate that the step of holding includes preheating of the wafer while supporting the wafer with respect to the stage without mounting the wafer on the upper member of the stage. Additionally, new dependent claims 9-14 have been presented, which recite the feature that the step of mounting includes contacting a substantial portion of a surface of the wafer with a substantial portion of the surface of the upper member of the stage and holding the wafer on the upper member of the stage while enabling plasma processing of the wafer. Further, the newly added dependent claims recite the feature of preheating of the wafer while supporting the wafer with respect to the stage without mounting the wafer on the upper member of the stage suppresses damage of the wafer due to a temperature difference between the wafer and the stage. Also, new dependent claims 13 and 14 relate to the supply of the cooling gas to the buffer room so as to effect cooling of the wafer. These features are clearly described in the specification of this application, and applicants submit that the claims, as amended, patentably distinguish over the cited art as will become clear from the following discussion.

At the outset, applicants note that the present invention is directed to the problem of thermal shock as described in connection with Figs. 14 and 15 of the drawings of this application, wherein as indicated at page 27, lines 5 et. seq., when a

semiconductor wafer is processed at a high temperature such as 500°C, rapid heat-up of the semiconductor wafer can result in occurrence accidental cracking due to application of thermal shocks. Therefore, in accordance with the present invention, when transferring a new wafer to be processed within the vacuum chamber, the wafer is transferred to a position corresponding to the upper member of the stage and is held at such position for a predetermined time period without mounting the wafer on the upper member of the stage, wherein the wafer is preheated by such positioning, and after the predetermined time expires, the wafer is then mounted on the wafer stage, as represented by steps 11, 12 and 13 in Fig. 15 of the drawings of this application. That is, as shown in Fig. 14, the temperature rise characteristic of the semiconductor wafer varies in units of wafer temperature and a time constant ("t" seconds) per wafer stage temperature is determinable from viewing this diagram. That is, in case of mounting a wafer on a stage which is provided with a heater within the upper member thereof and the upper portion of the upper member is heated to a high temperature, when a temperature difference is large between the wafer and the upper surface of the upper member of the stage, the wafer may be cracked or the thin film to be processed formed on the wafer may be damaged. When such a damaged wafer is processed, desired processing result cannot be obtained so that damage is detected for the first time after the wafers have been processed and collected. Accordingly, it is required to perform a countermeasure that the damaged wafer is replaced by a new wafer to be processed and processing is performed again for a new wafer, which degrades the efficiency of the apparatus and the operating efficiency thereof.

In accordance with the present invention, prior to mounting the wafer on the upper member of the stage, the wafer is held with respect to the stage without mounting thereon for a predetermined time period so as to preheat the wafer by radiant heat from the stage in advance and the thus preheated wafer is then mounted on the stage and plasma processing is effected. Since the wafer is

preheated before being mounted on the stage, the damage of the wafer due to thermal shock can be suppressed. Applicants submit that such features as recited in the independent and dependent claims of this application are not disclosed in the cited art as will become clear from the following discussion.

The rejection of claims 3-8 under 35 U.S.C. §103(a) as being unpatentable over Ishii (US 5,581,298) in view of Ushikawa (US 6,140,256) and Ratliff et al (US 6,492,621) is traversed insofar as it is applicable to the present claims, and reconsideration and withdrawal of the rejection are respectfully requested.

As to the requirements to support a rejection under 35 U.S.C. 103, reference is made to the decision of In re Fine, 5 USPQ 2d 1596 (Fed. Cir. 1988), wherein the court pointed out that the PTO has the burden under §103 to establish a prima facie case of obviousness and can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. As noted by the court, whether a particular combination might be "obvious to try" is not a legitimate test of patentability and obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. As further noted by the court, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.

Furthermore, such requirements have been clarified in the recent decision of In re Lee, 61 USPQ 2d 1430 (Fed. Cir. 2002) wherein the court in reversing an obviousness rejection indicated that deficiencies of the cited references cannot be remedied with conclusions about what is "basic knowledge" or "common knowledge". The court pointed out:

> The Examiner's conclusory statements that "the demonstration mode is just a programmable feature which can be used in many different device[s] for providing automatic introduction by adding the proper programming software" and that "another motivation

> would be that the automatic demonstration mode is user friendly and it functions as a tutorial" do not adequately address the issue of motivation to combine. This factual question of motivation is immaterial to patentability, and could not be resolved on subjected belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher."... Thus, the Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion. (emphasis added)

In applying Ishii to the claimed invention, the Examiner recognizes that:

> Ishii does not disclose a method comprising the steps of "transferring the wafer to a position corresponding to the upper member of the stage, holding the wafer at the corresponding position for a predetermined period, and mounting the wafer on the upper member", step of holding includes preheating the wafer, transferring the wafer to a buffer room to be cooled after processing, and transferring out of the buffer room. (emphasis added)

The Examiner contends that Ushikawa and Ratliff et al overcome such deficiencies of Ishii, and applicants submit that the Examiner has engaged in a hindsight reconstruction attempt of the present invention utilizing the principle of "obvious to try" which is not the standard of 35 U.S.C. §103, see In re Fine, supra, with the additional cited art failing to overcome the deficiencies of Ishii as discussed below.

Turning to Ushikawa, applicants note that this patent discloses a work table 3 in which the upper surface of the work table functions as a mount surface (3a) for mounting a wafer. The work table 3 includes two sets of vertical lifter pins including a first support means (4) having three vertical lifter pins (41, 42, 43) and a second support means (5) having three vertical pins (51, 52, 53). As described in connection with Figs. 6A-6E of Ushikawa, the wafer is transferred by the transfer arm 71 onto the second support means 5 so as to be supported on the lifter pins thereof which project from the mount surface 3a as shown in Fig. 6A, and upon withdrawal of the transfer arm 71, the lifter pins of the second support means 5 are moved

downwardly such that the wafer is mounted on the mount surface 3a of the work table 3 as described in col. 5 of Ushikawa. As indicated in col. 5, lines 30-45 of Uchikawa, the wafer while mounted on the mount surface 34 is heated to a process temperature by means of heat conduction through the mount surface 3a while the bottom surface of the wafer W is in plane-contact with the mount surface 3a of the work table 3, as shown in Fig. 6C. Thereafter, the wafer W is moved up by the first support means 4 so that the wafer W is not mounted on the mount surface 3a as shown in Fig. 6D at which position, the wafer is in a process position and processing is effected as described at col. 6 of Ushikawa. Thereafter, the wafer is transferred in the manner indicated in Fig. 6E. While the Examiner apparently contends that the operation of Ushikawa as represented by Figs. 6A and 6B, discloses transferring the wafer to a position corresponding to the upper member of the stage and holding the wafer at the corresponding position for a predetermined period, applicants submit that there is no disclosure in Ushikawa for holding the wafer at the position for a predetermined time period. Rather, Ushikawa specifically discloses that upon withdrawal of the transfer arm, the lifter pins are moved downwardly so as to mount the wafer on the mount surface 3a. Thus, applicants submit that Ushikawa fails to disclose or teach holding the wafer at the position corresponding to the upper member for a predetermined time period, which step of holding includes preheating of the wafer. Applicants submit that Ushikawa does not disclose preheating of the wafer in such position. Furthermore, while Ushikawa discloses mounting of the wafer on the mount surface 3a, in accordance with the disclosure of Ushikawa, such mounting is for preheating the wafer by contact of the wafer with the mount surface 3a, and after the preheating is effected, the wafer is moved away from contact with the mount surface 3a so as not to be mounted on the mount surface 3a to a position where processing of the wafer is effected in the manner illustrated in Fig. 6D of the drawings of this application. Thus, with respect to the features of independent claims 3 and 6, Ushikawa does not disclose or teach mounting of the wafer on the

upper member of the stage so as to enable processing of the wafer which is mounted on the upper member of the stage by using the plasma in the vacuum chamber as recited in such claims. Accordingly, applicants submit that the combination of Ushikawa and Ishii represents a hindsight reconstruction attempt with Ushikawa disclosing an operation which is diametrically opposed to that recited in independent claims 3 and 6 and the dependent claims of this application.

Applicants submit that it is apparent that Ushikawa does not process the wafer while the wafer is mounted on the mount surface 3a thereof. Additionally, Ushikawa fails to disclose holding the wafer at the position corresponding to the upper member of the stage for a predetermined time period without mounting the wafer on the upper member of the stage and effecting preheating as recited in dependent claims 4 and 7. Also, it is apparent that Ushikawa taken alone or in combination with Ishii, while disclosing mounting of the wafer on the mount surface 3a thereof, fail to disclose such mounting after preheating of the wafer and effecting the processing while the wafer is mounted on the mount surface 3a thereof. That is, in Ushikawa, the wafer after being preheated on the mount surface 3a, is lifted above the mount surface and held for a time so as to uniformly disperse heat over the entire surface of the wafer, at which time a film forming process is effected in the lifted position of the wafer. Furthermore, it is readily apparent that the heating of the wafer on the mount surface 3a in Ushikawa results in the high rise in temperature in the wafer and applicants submit that thermal shock occurs which is to be suppressed by the method of the present invention, which is not disclosed or taught by Ushikawa and Ishii taken alone or in any combination thereof. Thus, applicants submit that all claims patentably distinguish over this proposed combination of references.

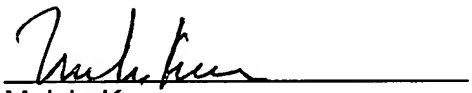
The Examiner has additionally utilized Ratliff et al for disclosing cooling of a wafer within a buffer room and applicants submit that the Examiner has mischaracterized the disclosure of Ratliff et al. Irrespective of the disclosure of Ratliff et al, applicants submit that this patent does not overcome the deficiencies of the

combination of Ishii and Ushikawa as pointed out above, and the combination again represents a hindsight reconstruction attempt utilizing the principle of "obvious to try". Furthermore, applicants submit that Ratliff et al does not disclose supplying a gas to the buffer room for cooling of the wafer which gas is a nitrogen gas, as described herein. Thus, applicants submit that independent claims 3 and 6 and therewith the dependent claims patentably distinguish over this proposed combination of references in the sense of 35 U.S.C. §103 and all claims should be considered allowable thereover.

In view of the above amendments and remarks, applicants submit that all claims patentably distinguish over the cited art and should now be in condition for allowance. Accordingly, issuance of an action of a favorable nature is courteously solicited.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (500.41374CX2) and please credit any excess fees to such deposit account.

Respectfully submitted,



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